Business

XConn's mission is to accelerate AI computing in data centers and high-performance computing (HPC) with their high

> *"As a result of this successful project and to extend our leadership, we are engaging with Synopsys on our future technology needs, including CXL 3.0 IP, for our next CXL switch SoC."*
>
> ~Gerry Fan, CEO, XConn

To build such high-capacity SoC, while achieving timing closure at 1GHz, XConn needed the technology and expertise of an IP provider that offered available, feature-rich IP on their target FinFET process node. After evaluating other IP products, XConn selected Synopsys' CXL 2.0 Controller and PCIe 5.0 PHY IP.

"Our aim was to provide the world's first CXL 2.0 switch SoC with the largest capacity in the market," said Fan, CEO. "To achieve such big task, we acquired Synopsys' high-quality CXL and PCIe IP after evaluating other products. We felt more comfortable with Synopsys IP because of the wide adoption, overall better performance, better latency and power, all of which led to much less design risk."

High-Quality Synopsys IP

Synopsys has been delivering high-quality IP for decades, actively participating in standards organizations to define and develop interface protocols such as PCIe and CXL. The IP supports all required features of the PCIe (1.0 to 6.0) and CXL (1.0 to 3.o) specifications. Synopsys introduced the world's first CXL controller, PHY and verification IP solutions, and has been the leading provider of PCIe IP across all the generations. Due to these reasons and many more, XConn was able to achieve first-pass silicon success and deliver their CXL 2.0 switch SoC to the market before anyone else.

XConn enjoyed valuable contributions that Synopsys IP brought to their projects, such as availability, the fact that the IP was proven and offered advanced features such as low-latency, low-power and high-throughput. The PHY offers x1, x2, x4, x8, x16 lane configurations supporting bifurcation, and lane margining at the receiver.

"We specifically liked the Synopsys CXL controller's Reliability, Availability and Serviceability (RAS) feature. It gave us the assurance we needed to maintain a high level of quality and reliability," said Fan. The RAS data protection provides error correction code (ECC) and/or parity protection for internal busses and memories.

"The Synopsys CXL 2.0 Controller IP supporting the PCIe 5.0 specification gave us assurance that the controller worked as intended while successfully interoperating with the PCIe 5.0 PHY IP," said Fan.

Expert Technical Support

XConn leveraged Synopsys' dedicated team of engineering experts to get the required to help with the 1GHz timing closure. "We received regular support from the Synopsys engineering team, helping us achieve our target timing closure and silicon success," said Fan. "Synopsys' expert technical support helped to integrate the IP in a timely manner."

Future Product Development

As a result of this successful project, XConn is engaging with Synopsys and discussing future technology needs, including CXL 3.0 IP, for their next generation switch SoCs.

> *"The dedicated assistance of Synopsys' expert technical support helped us close timing and achieve silicon success in the intended short timeframe."*
>
> ~Gerry Fan, CEO, XConn

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